



DSM presents: ForTii[®], the best fit for DDR4 housings

The global trends towards cloud computing, virtualization and high-performance computing demand for higher-performing, higher-density memory in computers.

Virtual servers enable operators to run multiple applications on a single instead of multiple servers. Such servers require a higher processor speed and higher memory density. The various applications running on such servers have different requirements: high-end servers used by enterprises to run large databases or process transactions require a large memory capacity with high reliability. Mid-end servers used for virtualization or data consolidation mainly require high bandwidth. Lower-end web servers, collaboration and infrastructure systems are essentially focused on low power, low cost and small form factor. Enterprises of all sizes from telecom to consumer electronics are increasingly challenged by rising energy costs and the need to improve their environmental footprint. A server running a virtualized environment delivers a higher utilization rate, but in turn demands for higher power.

In electronics Green Design has gained significant focus and will remain a hot topic for the upcoming years. Besides reduction of consumed energy, OEMs are increasingly restricting the use of certain halogens as flame retardant substances in plastics used e.g. in connector housings. The

memory that supports next-generation, Green Design must meet the diverse demands of higher performance, increased density, improved reliability, low power consumption and avoidance of (potentially) hazardous materials.

Market penetration of DDR4, the latest generation of computer memory will start in 2014: manufacturer are preparing for a move from DDR3 to DDR4 by the end of first quarter.

In this paper, the development of various halogen free DDR4 sockets is investigated and different options for the housing material are being technically discussed considering the much more stringent (Joint Electron Engineering Council) JEDEC DDR4 specification as well as the (International Electrotechnical Commission) IEC 61249-2 for halogen free compliance. We will benchmark various high performance polymers such as Liquid Crystal Polymers, Polyamide 4T, and different Polyphthalamides and highlight their performance with respect to key parameters such as connector reliability, pin retention forces, warpage or CTE match to the PCB.

DDR4 memory will first appear in servers, where OEMs are aggressively looking to lower power consumption while boosting performance. Around Q4 2014 then also initial high end desktop and gaming platforms will be launched with DDR4. While the actual memory modules are ready for mass production since last year, the required DDR4 sockets for the assembly of the module on the PCBs are just now being prepared for up-scaling.

DDR Evolution

Processors are using system memory to temporarily store the operating system, running applications and data they work on. The application reliability and performance is intrinsically tied to the bandwidth and speed of memory. This drove the evolution of memory from asynchronous DRAM technologies and Extended Data Out (EDO) memory, from 2000 onwards to high-bandwidth synchronous DRAM (SDRAM) technologies. However, bandwidth could never keep up with improvements in processors. As such the processor remains idle while reading data from the memory and the system running overall less efficient. To reduce the gap, the industry continuously pushes new memory technology developments. Various players across the value chain of the electronics industry work with JEDEC to ensure that new memory fulfills their needs for performance, reliability, cost and backward compatibility.

Published in September 2012, the initial JEDEC DDR4 (JESD79-4) standard has been defined to boost performance and reliability, while reducing durability, height and footprint, thereby representing a significant improvement over previous DRAM memory technologies.

By end of Q1 2014 first servers are expected to be introduced based on the new Intel Haswell E processors which is fully supporting the DDR4 standard. DDR4 will replace the current state of art DDR3 and DDR3L (low power version).

Since memory capacity is inversely proportional to the memory cell size, shrinking of the cell size leads to capacity increase. Originally, memory operating voltage was 5V. As cell size shranked , such voltages would burn the transistor gates. The latest DDR4 technology operates now at 1.2V, which allows a higher speed and less power consumptions.

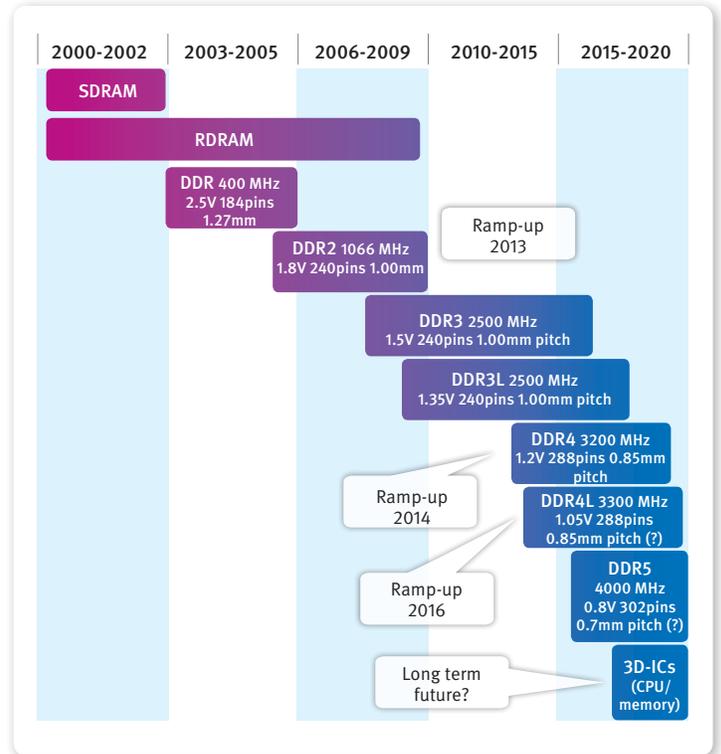
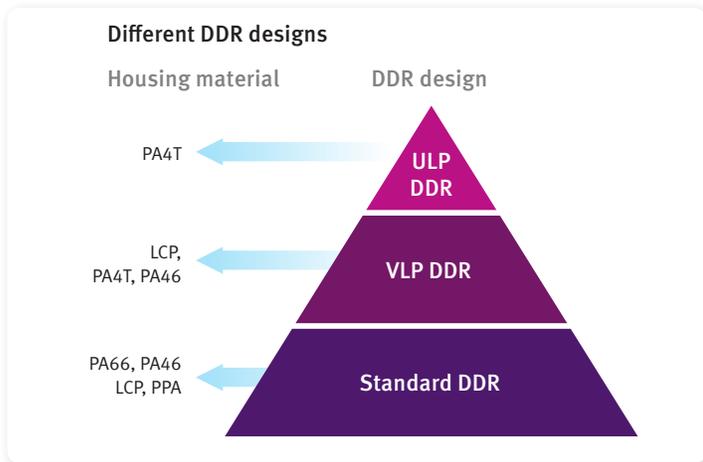


Figure 1: DDR development roadmap

- Thinner servers require smaller DDR memory heights to overcome
- space limitations
 - improve thermal performance by maximizing airflow over and through the DIMMs
 - enable easier rework



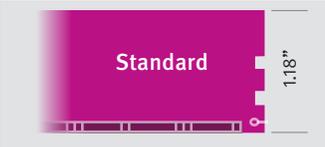
JEDEC height specifications	connector height	seating height of module
 0.70"	19.9 mm	2.1 mm
 0.738"	20.6 mm	2.3 mm
 1.18"	23.1 mm	3.12 mm

Figure 2: Different DDR design

Thin profile of VLP and ULP requires higher flowing, reflow capable materials. Low seating heights will bring LCPs to mechanical limits, SMT design to warpage limits! The first DDR4 modules were manufactured by Samsung and announced on September 2011. Since then an increased focus on required DDR4 sockets started at connector manufacturer.

DDR4 drives higher speed at reduced power consumption

DDR4-based modules of leading manufacturer such as Samsung or Micron are 20nm notch Semiconductor process and are available initially at 2.400Mb/s speed, increasing up to the full 3.200Mb/s as defined by JEDEC. Available modules will cover the density range between 8-128GB. DDR4 will provide computers with significantly improved power management and increased speed and performance. Compared to DDR3, DDR4 provides a 35% reduction in power consumption. With its Deep Power Down option combined with single memory chip refresh, rather than the entire module refresh in DDR3, DDR4 will also enable a 40-50% reduction in standby power. This significant power

reduction will reduce heat in every device that has access to the memory.

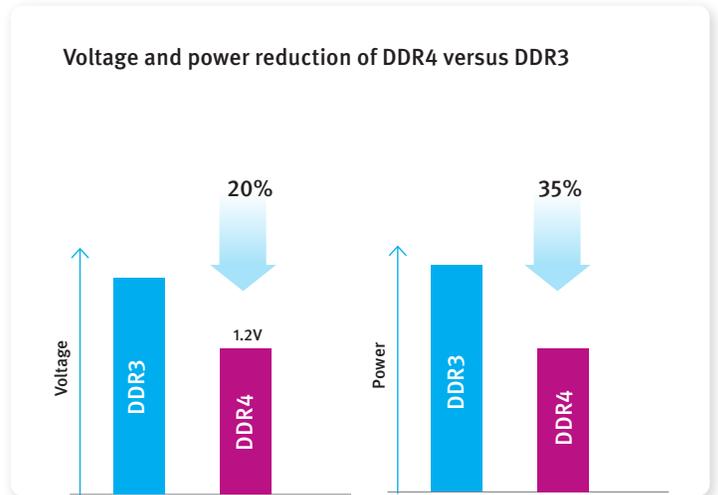


Figure 3: Voltage and power reduction of DDR4 versus DDR3

At the same time, DDR4 is far faster than anything before it. With 3.2 billion transfers per second, data transfer rates are double those of top-end DDR3 memory buses. During the initial phase, data transfer rates of DDR4 and DDR3 will overlap, while DDR4 will then gradually evolve to its full speed of 3.200Mb/s until even faster DDR4L generation will speed up further.

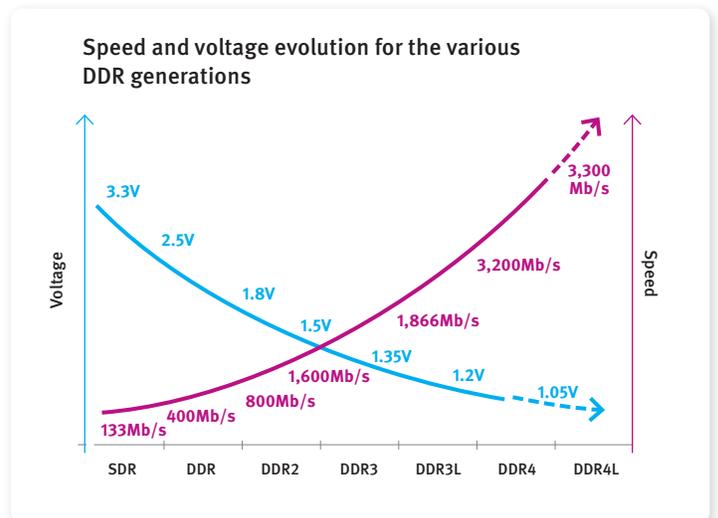


Figure 4: Speed and voltage evolution for the various DDR generations

DDR4 versus DDR3 Specification

DDR4 shows across the boards improvements over DDR3. OEMs can achieve a significant performance improvement.

Benchmark of current, mainstream DDR3 versus latest generation DDR4

Feature	DDR4	DDR3	Advantage DDR4 over DDR3
Core and I/O Voltage	1.2V	1.5V	20% voltage reduction, heat reduction in devices with memory access
Low voltage standard	Planned, likely 1.05V	Yes, DDR3 at 1.35V	Further power reduction
Data rate [Mb/s]	1600 - 3200	80 - 2133	Higher speed I/O
Densities [GB]	2 - 8	0.512 - 8	Larger memory capacity
Memory banks	16	8	More banks
Bank groups	4	0	Faster burst rates
Overclock DLL enabled	667 MHz - 1.6 GHz	300 - 800 MHz	Higher data rates
R _{TT} values in Ω	240, 120, 80, 60, 48, 40, 34	120, 40, 40, 30, 20	Support higher data rates
Memory refresh	Entire memory refresh + entire power down	Single memory refresh	40-50% standby power reduction, heat reduction in devices with memory access
Data transfers per seconds	Up to 3,2 billion	Up to 1,6 billion	Double data transfer rates
Module thickness [mm]	1.40	1.27	10% increase (still to fit in narrow socket)
Pitch size [mm]	0.85	1.00	15% reduction
Pin count	288	240	20% more pins
Designs	VLP and ULP	Standard, VLP and ULP	Smaller module height
Total max. socket length [mm]	142	141	No change length
Total max. socket width [mm]	7.75	6.5	Reduced connector footprint
SMT pad width [mm]	0.57	0.7	19% reduction
PTH Via diameter [mm]	0.66	0.7	6% reduction of Via diameter

Table 1: Benchmark of current, mainstream DDR3 versus latest generation DDR4

Material benchmark

The required high performance and quality of DDR4 poses challenging requirements to the housing material of the connectors. In this article we compare five high performance materials on the requirements as described above: LCP, PPA, PA4T, PA46 and PA66.

DDR4 requirements and material needs

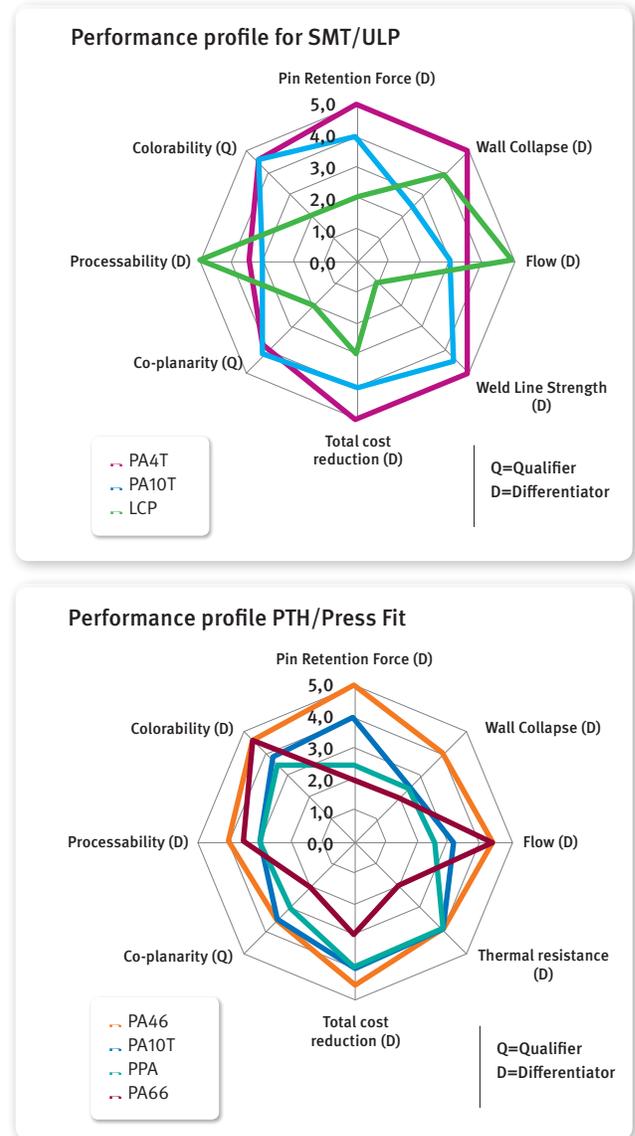


Figure 5: DDR requirements and material characteristics summarized for various option

Figure 5 (up) shows the materials tested SMT and ULP DDR4 connectors. No blistering during reflow soldering and excellent co-planarity are the two key qualifiers (Q). A material not performing sufficiently good in these two criteria excludes its use in DDR4. These two designs require housing plastics of highest temperature and mechanical performance. Figure 5 (down) shows the same view for the

PTH and Press fit designs. Key qualifiers are no blistering at wave soldering and excellent co-planarity. Somewhat less critical design parameters are the so called differentiators (D). These parameters don't exclude the use of a certain material in the application. If there are multiple materials available fulfilling the qualifiers, manufacturers make their material choice based on the broadest balance of differentiators, bottom line enabling highest productivity and lowest total cost.

Methods of DDR4 Termination

Termination is a key concept in connector design. It refers to the method used to join a terminal and a conductor. Good termination assures sound electrical contact and maximum strength between the conductor and the terminal (for a gas-tight connection, to prohibit corrosion). The common termination methods used for DDR4 are

- Surface mount (will be the trend in the future and already now applied on servers of e.g. Oracle or IBM)
- Pin Through Hole (currently mainstream technique, mostly applied in desktops)
- Pin-in Paste (used mainly in All-In-One PCs)
- Press fit (used in mainly in Telecom)

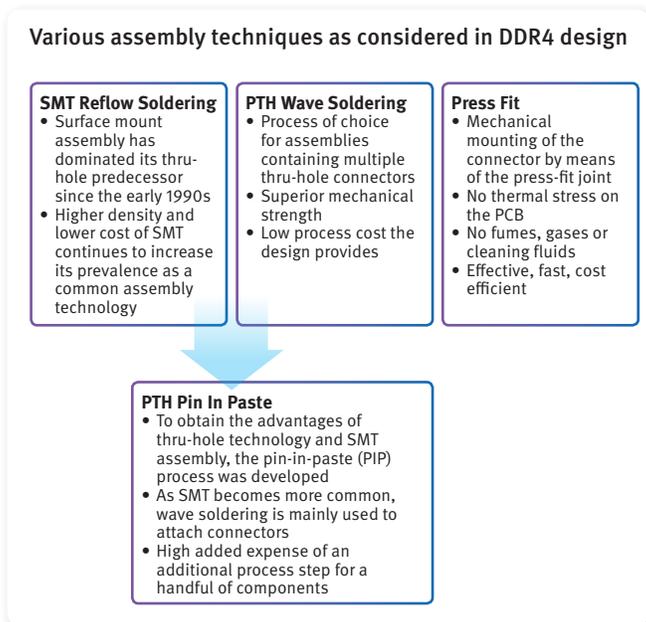


Figure 6: Various assembly techniques as considered in DDR4 design

Depending on the OEM and specifics of the board design such as numbers of PCB layers, one of the above DDR4 connector types can be applied. Details of the connector design differ and for this paper most relevant, the choice of the housing material is directly triggered. For Pin-In-Paste

and SMT design very high temperature plastics are a must because of the applied reflow soldering step during assembly. Fully complying with RoHS, the connector is exposed to lead free assembly temperatures in the range of 260-280°C, including some local hot spots. Materials of choice must have extreme mechanical and thermal properties to withstand such high temperatures where the peak temperature is present for approx 10secs. Furthermore, materials must show a proper balance of low moisture absorption and high surface tension. This avoids the formation for so called blisters which can appear during high, IR-reflow processing temperatures if the wrong material is selected or if the processing conditions during connector manufacturing or connector storage are not properly set.

Such above requirements are somewhat less critical for the PTH design where the actual PCB is acting as a kind of heat shield during assembly. The effective temperature exposure of the connector housings is therefore about 15°C lower than in the case of reflow soldering.

Pin-In-Paste is somewhat a combination of reflow and pin through hole connector design. While the pins go through the hole, the actual assembly is still done in a reflow process. The advantage of this is that PCBs can be exposed to only one reflow process, rather than sending them first through a reflow step to assemble most of the ICs and discrete components followed by an adjacent wave soldering step for the bulkier connectors. Such temperature exposure is not present during press fit assembly. So in principle various low temperature plastics could be used as well. However, since most OEMs have multiple designs and often they prefer to use components such as DDR connectors on all these designs without extra selection effort, the bottom line cost and design / supply chain flexibility is highest if high temperature plastics are also selected for press fit design.

Connector warpage

Warpage of a connector happens when the connector is losing its co-planarity while being soldered onto a Printed Circuit Board (PCB). Such warpage is a complex phenomenon and driven by various parameters such as the heat distortion temperature (HDT) of the insulation material used for the connector housings, the difference of comparative thermal expansion (CTE) between the plastic body and the PCB, the flow of the housings material and related stress incorporated during injection molding of the connector housings.

CLTE (coefficient of linear thermal expansion)

To achieve good co-planarity of the connector on the FR4 or latest halogen free printed circuit boards (PCBs), there has to be a close match in CLTE between the board and the connector housing material. In addition, a combination of high stiffness and high deflection temperature under load (HDT) is required to ensure low warpage after reflow soldering .

Flow

Producing good quality DDR4 connectors while keeping cost to OEMs affordable, manufacturer strive for housing materials with highest possible flow while meeting key design requirements such as mechanics, coplanarity or color ability. A high flow equals high number of cavities during the injection molding process. At the same shot of the injection molding machine therefore more housings can be produced which correlates directly with manufacturing cost. A high flow at the same time also leads to less incorporated stress in the housing. Such a stress relaxes at the higher temperature exposure during connector assembly. As a consequence the connector will then warp and specifically signal pins at both ends of the connector may lose their electrical contact to the PCB. Such warpage leads to either fatal errors during board assembly, or in the worst case may even result in field return if such a contact can become loose after some time under the continuous impact of tension between PCB and connector. In either way it involves high repair cost which can easily outpass manufacturing cost of the actual connector by manifold.

Traditionally, when a molder or connector manufacturer is looking for high flowing materials, LCPs (Liquid Crystal Polymers) are often the material of choice.

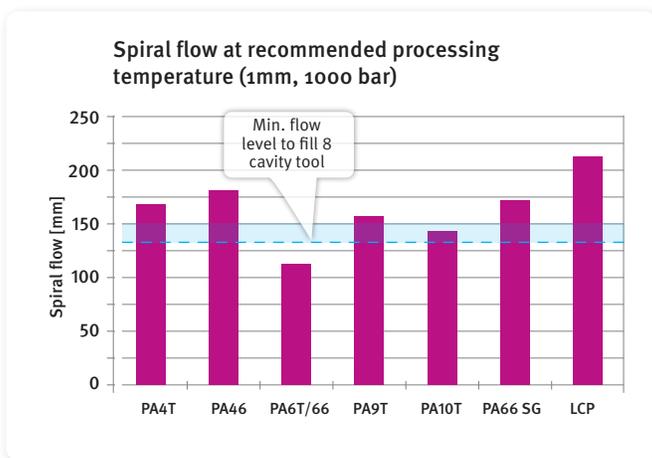


Figure 7: Flow of various insulating materials

Figure 7 shows the flow length of various materials tested in DDR4 connectors. The higher the flow levels, the easier it is to fill the mold cavities and the more cavities can be used during molding. The red bar indicates minimum flow levels to enable 8-cavity design for a PTH housing and 4 cavities for a ULP or SMT housing. Materials which are below the blue bar or have only little margin, will either not allow high cavity mold design or will lead to significant processing issues later on during mass production of the connectors. Molders in such a case would traditionally increase the processing temperatures so that the viscosity of the materials in their liquid phase increases. While this will indeed lead to an observed flow improvement, materials are often treated outside their ideal processing windows leading

to high outgassing and material degradation. This can as secondary effect result in so called blisters of the housing during assembly or can reduce molding throughput and therefore lead to extra cost. From flow perspective, LCPs show the best performance, followed by PA46, PA66 and PA4T.

While LCPs are indeed excellent in flow and have also done an acceptable job up to the generation of DDR3, from DDR4 onwards all LCPs are failing in warpage. The reason is the significantly higher design complexity, the thinner walls, smaller width and height and the higher pin count of DDR4 connectors. Figure 8 shows the warpage of a DDR4 connector before and after assembly, on the top side for LCP on the bottom side for PA4T and PA46. Upon molding the warpage is looking comparable for either housing material. After assembly to the PCB however, LCP housings show a significant warpage with a flip in direction (“crying phase becomes a smile”). The delta in warpage before and after assembly can easily be 0.5mm and higher. More critical than the actual warpage is the often observed change in warpage direction which makes any prediction and warpage correction in the design literally impossible. LCP material suppliers have reacted and evolved LCP compounds to newer LCP/PPS blends. The higher stiffness of PPS leads to some improvement in warpage and allowed the use of such blends in DDR3 while in return resulting in significant processing issues. In DDR4, however, also these blends are not meeting the required co-planarity levels.

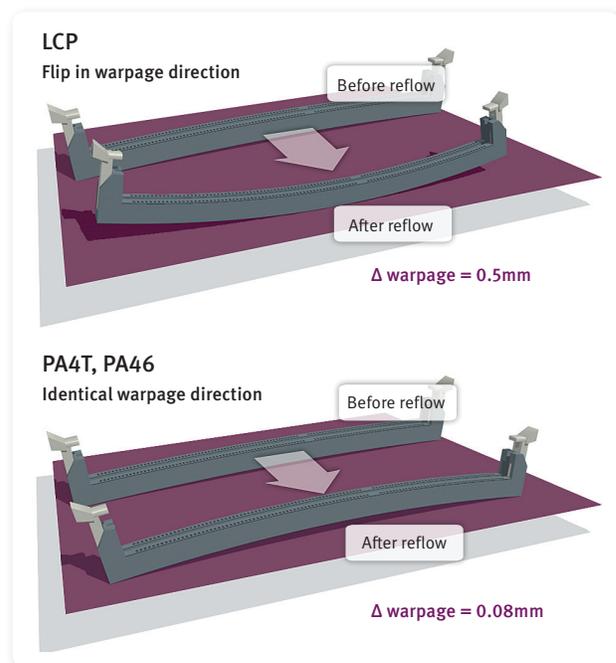


Figure 8: Impact of warpage on a DDR connector soldered on a PCB

At the bottom of Figure 8 the same case is shown for DDR4 housings based on Polyamides 4T and 46. The warpage after assembly is significantly lower and well below the 0.1mm specification. Moreover, both polyamides do not show any

flip in direction, enabling good prediction and additional correction of warpage to connector designers. A key driver for warpage is the so called HDT (Heat Deflection Temperature) of the used housings material.

Heat Distortion Temperature (HDT)

HDT defines the temperature where the polymer becomes soft and can start to deform. Figure 9 shows HDT-A (1.8MPa) of various materials which have been tested for the upcoming DDR4 connectors. The blue bar indicates a range of HDT which is border line for good warpage performance during the assembly process of connector assembly. Materials with lower HDT cannot be used at reflow soldering, materials with HDT inside the blue bar show border line performance and require huge design and manufacturing efforts such as mechanical fixation by clamps during assembly). Material with an HDT above the blue bar are on the save side and show low warpage even without any fixation to the board. Such low warpage does not only increase assembly speed, quality and reliability of the boards, but furthermore also lead to lowest assembly cost at the molder as the additional mechanical fixation step and the required tools for this can be omitted.

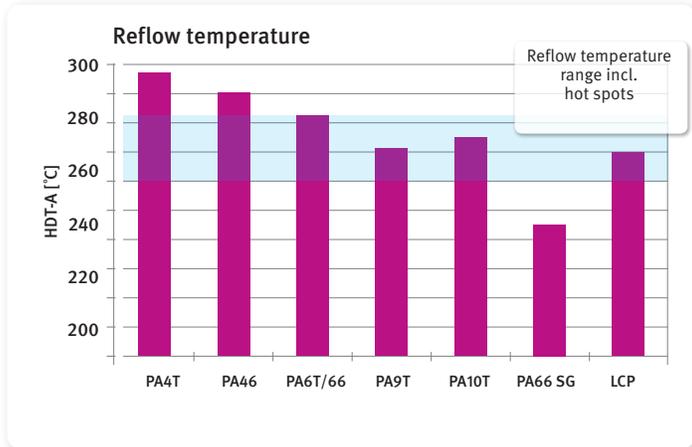


Figure 9: HDT-A (1.8MPa) of various polymers. The temperature range highlighted in blue is required in order to enable low warpage and to avoid that the side walls of the connector collapse

It is therefore required to use plastic materials with a high HDT, especially covering also temperatures which could be present in hot spots during the soldering process. Only PA46 and PA4T have high enough temperatures ranges to show high reliability also during reflow soldering assembly.

HDT also has a very important role on the reliability of a DDR4 connector. A too low HDT would enable the side walls of the connector to slightly collapse during assembly on the PCB. This collapse will increase the required memory module insertion and removal forces. During insertion or removal of the socket in the worst case cracks could occur at the thin parts of the connector or the number of insertion/removal cycles can be drastically reduced. Figure 10 shows such a collapse of the side walls.

Pin retention force

Pin retention (to Housing Contact retention) force holds a terminal in a housing cavity. This prevents terminal back-out, or the coming loose of the terminal. Typically, locking devices called tangs secure the terminal against the housing walls using spring-like pressure. The contact retention to housing specification describes the force required to remove a properly seated terminal.

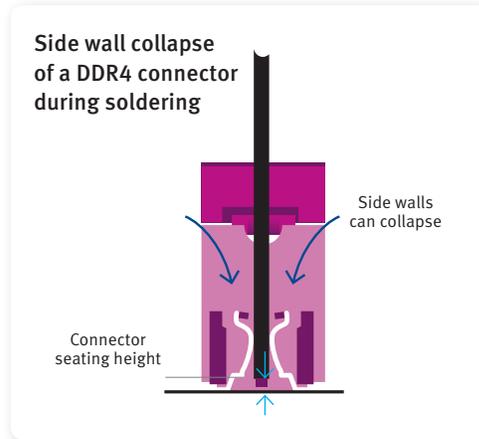


Figure 10: Side wall collapse of a DDR4 connector during soldering if the HDT of the insulation material is too low

Reduction of pitch size from 1mm in DDR3 to 0.85mm in DDR4 increases the challenge for pin retention forces (DDR4 requires at least 0.3kgf/pin). Since memory connectors are specified for approx. 25 insertion/removal cycles (see Figure 11 left), a high pin retention force is essential for the quality and reliability of the connector and entire board later on during its use phase in the field (see Figure 11right). Upon removal of memory module the connector housings must firmly be attached to the pins. Too low pin retention forces can lead to fatale failure modes resulting in very expensive and reputation damaging field returns of OEMs. Especially in the professional field of servers which are being used e.g. in telecom or in the financial sector, such failures are totally unacceptable and manufacturer will plan for even higher extra margins to guarantee long live times of 5-10 years.

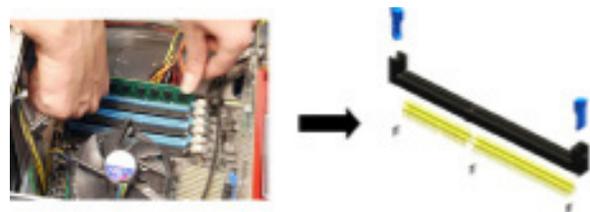


Figure 11: Too low pin retention forces can lead to fatale failure mode

Pin retention forces depend a lot on the type of housing materials used, but is also strongly influenced by connector and pin design. The ULP (Ultra Low Profile) design for instance allows a wider material tolerance on pin retention forces since the design allows a large compensation. Such flexibility in the case of pin through hole design is less, the proper choice of the plastics for the housing becomes key to connector quality and reliability.

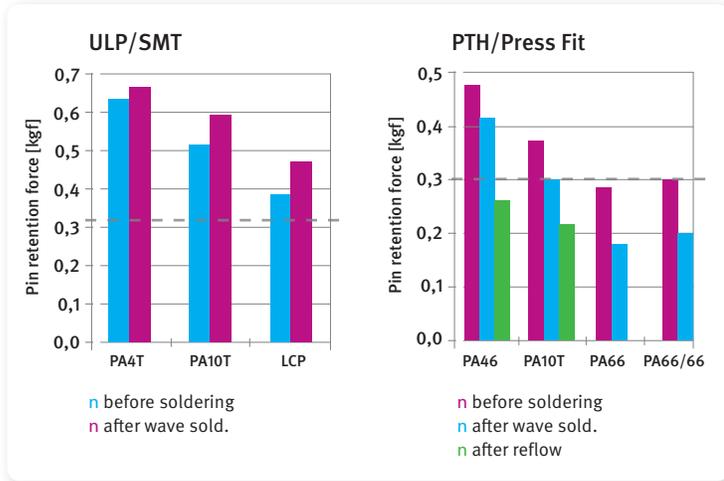


Figure 12: Pin retention forces of various insulating materials before and after soldering exposure. Materials for SMT and ULP design (left) and material for PTH and press fit design (right)

Figure 12 shows the outstanding performance of PA4T for ULP and SMT design with highest possible pin retention forces before and after soldering. For the pin retention forces of PTH connectors, PA46 has been found best in class keeping the required 0.3kgf/pin after soldering also after soldering. Other materials such as PPAs (PA10T, PA6T/66) or PA66 may still be okay during connector assembly, but show a strong decay below the specified 0.3kgf/pin. With such materials quality and reliability is jeopardized and the risk for high rejects at assembly or field returns in the use phase is high. The cost/performance ratio is not justifying the use of these materials for DDR4.

Conclusions

The polyamides PA46 and PA4T are the current material of reference in various DDR1-DDR3 designs. For the successful development of the new generation DDR4, not only a deep solid understanding of the application and material was required, moreover the close co-operation between the connector manufacturer as well as the material supplier in alignment with leading OEMs was essential.

The challenging design of DDR4 and the various changes from previous DDR3 technology have significantly increased the application requirement for mechanical strength, pin retention force and flow. Due to its outstanding combination of flow and mechanics, PA46 has been found the most suitable material for PTH and Press fit design. PA 4T with its

approx. 25°C higher melt temperature combined with a higher surface tension and a higher moisture resistance has been found the material of choice for SMT and ULP designs.

Warpage is already in DDR3 a key challenge in servers, with the increased move towards SMT, ULP and VLP design as well as growing number of DDR sockets per server board, the warpage challenge increases in future and can bend even entire PCBs. Both PA46 and PA4T are showing outstanding performance in co-planarity and significantly lower the risk of expensive PCB returns and rework. Warpage combined with the low mechanical strength disqualify LCPs from the upcoming DDR4 technology.

With the growing focus of the electronics industry on sustainability, this development has been focused to not only avoid any hazardous materials as per Directive 2011/65/EU RoHS, moreover it is also fully meeting IEC61240-2-21 compliancy for halogen free. While such halogen free flame retardancy is also required currently by some OEMs, the two polyamides PA46 and PA4T are ensuring full future compatibility and avoid any further requalification on the connector manufacturer neither on OEM side.

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